

Claims

What is claimed is:

- 5 1. A memory system comprising:
 a first memory controller;
 a first memory component;
 a first address and control bus connected to the first memory controller and the
10 first memory component; and
 a first data bus connected to the first memory controller and to the first memory
 component, wherein the first data bus uses differential signaling and has a first data bus
 symbol time that is shorter than a first address and control bus symbol time of the first
 address and control bus.
- 15 2. The memory system of claim 1 further comprising:
 a second memory component connected to the first address and control bus and to
 the first data bus.
- 20 3. The memory system of claim 1 further comprising:
 a second memory component connected to the first address and control bus; and
 a second data bus connected to the first memory controller and to the second
 memory component, wherein the second data bus uses differential signaling and has a
 second data bus symbol time that is shorter than the first address and control bus symbol
 time of the first address and control bus.
- 25 4. The memory system of claim 1 wherein a quotient of the first data bus symbol
 time divided by the first address and control bus symbol time is less than or equal to 1/8.

5. A memory system comprising:

a first memory controller;

a first memory component;

a first address and control bus connected to the first memory controller and to the

5 first memory component;

a first clock signal conductor connected to the first memory controller and to the first memory component; and

a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus has a first data bus symbol time that is shorter than

10 a first address and control bus symbol time of the first address and control bus and

wherein the first address and control bus symbol time is shorter than a first clock signal cycle time of the first clock signal.

6. The memory system of claim 5 further comprising:

15 a second memory component connected to the first address and control bus, to the first clock signal conductor, and to the first data bus.

7. The memory system of claim 5 further comprising:

20 a second memory component connected to the first address and control bus and to the first clock signal conductor; and

a second data bus connected to the first memory controller and to the second memory component, wherein the second data bus uses differential signaling and has a second data bus symbol time that is shorter than the first address and control bus symbol time of the first address and control bus.

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8. The memory system of claim 5 wherein a first quotient of the first data bus symbol time divided by the first address and control bus symbol time is less than or equal to $1/8$ and a second quotient of the first address and control bus symbol time divided by the first clock signal cycle time is less than or equal to $1/2$.

9. A memory system comprising:
a first memory controller;
a first memory component;
a first address and control bus connected to the first memory controller and to the
5 first memory component; and
a first data bus connected to the first memory controller and to the first memory
component, wherein the first memory component includes a first termination structure
connected to the first data bus and wherein the first data bus has a first data bus symbol
time that is shorter than a first address and control symbol time of the first address and
10 control bus.
10. The memory system of claim 9 further comprising:
a second memory component connected to the first address and control bus; and
a second data bus connected to the first memory controller and to the second
15 memory component, wherein the second memory component includes a second
termination structure connected to the second data bus and wherein the first data bus
symbol time is shorter than the first address and control bus symbol time of the first
address and control bus.
- 20 11. The memory system of claim 9 wherein the first memory controller includes a
third termination structure connected to the first data bus.
12. The memory system of claim 9 wherein a quotient of the first data bus symbol
time divided by the first address and control bus symbol time is less than or equal to $1/8$.
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13. The memory system of claim 9 wherein a calibration process is used to adjust a
first termination value of the first termination structure.

14. A memory system comprising:
a first memory controller;
a first memory component;
a first address and control bus connected to the first memory controller and to the

5 first memory component; and

a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus, wherein the first data bus uses differential signaling, and wherein the first address and control bus uses non-differential signaling.

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15. The memory system of claim 14 further comprising:

a second memory component connected to the first address and control bus; and
a second data bus connected to the first memory controller and to the second

memory component, wherein the second memory component includes a second

15 termination structure connected to the second data bus and wherein the second data bus uses differential signaling.

16. The memory system of claim 14 wherein the first memory controller includes a third termination structure connected to the first data bus.

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17. The memory system of claim 14 wherein a calibration process is used to adjust a first termination value of the first termination structure.

18. A memory system comprising:
a first memory controller;
a first memory component;
a first address and control bus connected to the first memory controller and to the
5 first memory component; and
a first data bus connected to the first memory controller and to the first memory
component, wherein the first data bus uses differential signaling and wherein the first
memory component accesses a first word stored in the first memory component, the first
word being wider than a first data bus width of the first data bus.
- 10 19. The memory system of claim 18 further comprising:
a second memory component connected to the first address and control bus and to
the first data bus.
- 15 20. The memory system of claim 18 further comprising:
a second memory component connected to the first address and control bus; and
a second data bus connected to the first memory controller and to the second
memory component, wherein the second data bus uses differential signaling and wherein
the second memory component accesses a second word stored in the second memory
20 component, the second word being wider than a second data bus width of the second data
bus.

21. A memory system comprising:
a first memory controller;
a first memory component;
a first address and control bus connected to the first memory controller and to the
5 first memory component; and
a first data bus connected to the first memory controller and to the first memory
component, wherein the first memory controller includes a first receive circuit having a
first read timing adjustment subcircuit for adjusting a first adjustable read data sampling
time point for first read data sampled from the first data bus and wherein the first data bus
10 uses differential signaling.
22. The memory system of claim 21 further comprising:
a second memory component connected to the first address and control bus; and
a second data bus connected the first memory controller and to the second
15 memory component, wherein the first memory controller includes a second receive
circuit having a second read timing adjustment subcircuit for adjusting a second
adjustable read data sampling time point for second read data sampled from the second
data bus and wherein the second data bus uses differential signaling.
- 20 23. The memory system of claim 21 wherein a calibration process is used to adjust
the first adjustable read data sampling time point.
24. The memory system of claim 21 wherein the first memory controller contains a
first transmit circuit having a first write timing adjustment subcircuit for adjusting a first
25 adjustable write data driving time point for first write data driven on the first data bus.

25. A memory system comprising:
a first memory controller;
a first memory component;
a first address and control bus connected to the first memory controller and to the
5 first memory component; and
a first data bus connected to the first memory controller and to the first memory
component, wherein the first memory controller component includes a first receive circuit
having a first read timing adjustment subcircuit for adjusting a first adjustable read data
sampling time point for first read data sampled from the first data bus and wherein the
10 first memory component includes a first termination structure connected to the first data
bus.
26. The memory system of claim 25 further comprising:
a second memory component connected to the first address and control bus; and
15 a second data bus connected to the first memory controller and to the second
memory component, wherein the first memory controller includes a second receive
circuit having a second read timing adjustment subcircuit for adjusting a second
adjustable read data sampling time point for second read data sampled from the second
data bus and wherein the second memory component includes a second termination
20 structure connected to the second data bus.
27. The memory system of claim 25 wherein a calibration process is used to adjust
the first adjustable read data sampling time point.
- 25 28. The memory system of claim 25 wherein the first memory controller includes a
first transmit circuit having a first write timing adjustment subcircuit for adjusting a first
adjustable write data driving time point for first write data driven on the first data bus.
29. The memory system of claim 25 wherein the first memory controller includes a
30 third termination structure connected to the first data bus.